

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT****Complete if Known**

Application No.	10/773,385
Filing Date	February 5, 2004
First Named Inventor	Donald S. Steiss
Art Unit	2183
Examiner Name	Eric Coleman
Attorney Docket Number	22347-08564

Sheet

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of

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U.S. PATENT DOCUMENTS

U.S. PATENT DOCUMENTS				
Examiner Initials*	Cite No. ¹	Document No. Number – Kind Code ² (if known)	Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
	A1	US-2002/0062435 A1	05-23-2002	Nemirovsky et al.
	A2	US-2001/0032307 A1	10-18-2001	Rohlman et al.

FOREIGN PATENT DOCUMENTS

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OTHER REFERENCES – NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ⁶
	C1	REGNIER, G., et al., "ETA: Experience with an Intel® Xeon™ Processor as a Packet Processing Engine," IEEE Proceedings of the 11 th Symposium on High Performance Interconnects, August 20-22, 2003, pp. 76-82.	

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